DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 and 10-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemirovsky et al., U.S. Patent No. 6,389,449 (hereinafter Nemirovsky).

3. Referring to claim 1, Nemirovsky has taught a method comprising:

in a processor based system where a plurality of logical processors *[The processor has a plurality of contexts (called streams), which are logical processors]* of a single physical processor *[one physical processor; See FIG. 1A]* share processor execution resources of the single physical processor *[Functional Resources; FIG. 1A, component 107]*, in response to a first logical processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduling tasks, making a processor execution resource previously reserved for the first logical processor available to any of the plurality of logical processors *[The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53). Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical processors)]*.

4. Referring to claims 2 and 21, taking claim 2 as exemplary, Nemirovsky has taught the method of claim 1 further comprising reserving the processor execution resource for the first processor in response to the first processor being scheduled to execute a task *[column 6, lines 33-47]*.

5. Referring to claims 3 and 22, taking claim 3 as exemplary, Nemirovsky has taught the method of claim 2 wherein each of the plurality of processors is a logical processor of the processor based system *[column 4, lines 48-60]*

6. Referring to claims 4, 11, 16, and 23, taking claim 4 as exemplary, Nemirovsky has taught the method of claim 3 wherein the first processor being scheduled to enter an idle state further comprises the

first processor executing a processor instruction requesting the first processor to enter an idle state *[the stream executes an instruction that puts it to sleep (i.e. idle); column 10, lines 55-64*

7. Referring to claim 5, 12, 17, and 24, taking claim 5 as exemplary, Nemirovsky has taught the method of claim 4 wherein making the processor execution resource previously reserved for the first processor available to any of the plurality of processors further comprises releasing the processor execution resource into a common pool of processor execution resources *[making the previously reserved resource available comprises modifying the resource assignment bitmap, thereby releasing the resource into a common resource pool; column 6, lines 29-47]*.

8. Referring to claims 6 and 25, taking claim 6 as exemplary, Nemirovsky has taught the method of claim 2 wherein the first processor being scheduled to execute a task further comprises the first processor receiving a wake up signal *[An idle thread receives a wake up signal from the supervisor thread to execute a task; column 10, lines 22-34]*.

9. Referring to claims 7, 13, 18, and 26, taking claim 7 as exemplary, Nemirovsky has taught the method of claim 6 wherein the processor execution resource previously reserved for the first processor further is statically allocated to the first processor *[column 6, lines 48-57]*; and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises de-allocating the processor execution resource from the first processor *[releasing the resource into a common resource pool comprises deallocating the resource using the resource assignment bitmap; column 6, lines 29-47]*.

10. Referring to claim 8, 14, 19, and 27, taking claim 8 as exemplary, Nemirovsky has taught the method of claim 6 wherein the processor execution resource previously reserved for the first processor is locked by the first processor *[reserved resources are indicated as locked by the resource assignment bitmap; column 6, lines 29-47]*; and wherein releasing the processor execution resource into a common pool of processor execution resources further comprises unlocking the processor execution resource processor *[releasing the resource into a common resource pool comprises unlocking the resource by modifying the resource assignment bitmap; column 6, lines 29-47]*.

11. Referring to claim 10, Nemirovsky has taught a processor comprising:

A single physical processor *[one physical processor; See FIG. 1A]* that implements a plurality of logical processors *[The processor has a plurality of contexts (called streams), which are logical processors]*; and logic to execute an instruction set which when executed by a first logical processor, cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors in response to the first logical processor being scheduled to enter an idle state due to lack of scheduling tasks *[The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53). Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical processors)]*.

12. Referring to claim 15, Nemirovsky has taught a system comprising: a physical processor *[one physical processor; See FIG. 1A]*, the processor comprising: a plurality of logical processors *[The processor has a plurality of contexts (called streams), which are logical processors]* implemented in the physical processor; and an instruction set, the instruction set comprising one or more instruction which when executed by a first logical processor, cause the first logical processor to make a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processor in response to the first logical processor being scheduled to enter an idle state due to lack of scheduled tasks *[The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53). Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical processors)]*; firmware to schedule the first logical processor to enter an idle state [the master thread is firmware (column 8, lines 15-30) thread that can put streams to sleep (i.e. idle) (column 7, lines 47-65)]; and a bus to interconnect the firmware and the processor *[See bus connecting instruction memory with processor; FIG. 1A]*.

13. Referring to claim 20, Nemirovsky has taught a machine accessible medium having stored thereon data which when accessed by a machine cause the machine to perform a method, the method comprising: in a processor based system where a plurality of logical processor *[The processor has a plurality of contexts (called streams), which are logical processors]* implemented in a single physical

processor *[one physical processor; See FIG. 1A]* share processor execution resources of the physical processor *[Functional Resources; FIG. 1A, component 107]*, in response to a first logical processor in the plurality of logical processor being scheduled to enter an idle state due to lack of scheduled tasks, making a processor execution resource previously reserved for the first logical processor available to a second logical processor in the plurality of processors *[The streams have reserved resources (See FIG. 1C; column 6, lines 41-46) and can change their resources according to their needs (column 9, lines 49-53). Therefore, when a stream is idle it makes the resources previously reserved for it available to the other streams (i.e. logical processors)]*.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 9 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky.

16. Referring to claims 9 and 28, taking claim 9 as exemplary, Nemirovsky has taught the method of claim 5 wherein the common pool of processor execution resources comprises a variety of processor resources [Nemirovsky; column 23-32]. Nemirovsky has not explicitly taught that the pool comprises a translation lookaside buffer and the processor execution resource is a translation cache entry from the translation lookaside buffer. However, it would have been obvious to one of ordinary skill in the art to modify Nemirovsky so that the pool of common resources would include a translation lookaside buffer and the resource would be a translation cache entry from the translation lookaside buffer. The motivation for doing so would have been to allow translation lookaside buffer entries to be shared among streams as needed.

Response to Arguments

17. Applicant's arguments filed 04/15/2011 have been fully considered but they are not persuasive.

18. The applicant argues the novelty/rejection of the claims, in substance, that "Nemirovsky does not disclose, teach, or suggest 'in response to a first logical processor in the plurality of processors being scheduled to enter an idle state due to lack of scheduling tasks, making a processor execution resource previously reserved for the first logical processor available to any of the plurality of logical processors'" as recited in independent claim 1 and similar limitations in independent claims 10, 15, and 20.

19. The applicant's first point regarding the above limitation is that the cited section of Nemirovsky (column 9, lines 49-53) discloses a stream manipulating its own resource allocation and priority, which the applicant believes "is not the same as 'being scheduled to enter an idle state due to lack of scheduling tasks.'" The cited section of Nemirovsky discloses that an "active stream may manipulate its own resource allocation and priority according to its needs, which will relate closely to the nature of the thread running in the stream, and the nature of other threads available to run or actually running in other streams." Nemirovsky further discloses a stream manipulates its resource allocation by reserving specific processor resources via resource assignment bits that indicate to other streams that either the resource associated with a particular bit is reserved (and therefore unavailable) or the it is not reserved (and therefore available. See Nemirovsky; column 6, lines 33-47. Therefore, when a stream becomes idle due to a lack of scheduling tasks and no longer needs a particular resource the stream will indicate that the resource is no longer reserved, thereby making the resource available to other streams.

20. The applicant's second point regarding the above limitation is that the Nemirovsky has not taught "logical processors." The applicant indicates in the background section of the specification that logical processor is a component of a processor that maintains its own architectural state, but that shares hardware resources. See e.g. paragraphs [01] and [02] in the background section. Similarly, the streams of Nemirovsky are processor components that maintain their own architectural state or context. See Nemirovsky; column 1, lines 65-66. It is unclear to the examiner in what way the applicant believes the streams of Nemirovsky are different from logical processors as disclosed in the applicant's specification.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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